

COS/MOS Rate Multipliers—Versatile Circuits for Synthesizing Digital Functions

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The RCA COS/MOS rate multipliers, CD4527B and CD4089B, are versatile MSI circuits that can be used as building blocks to generate a range of digital functions in low-power systems where minimum package count is desirable. Rate multipliers can be used in various applications, such as numerical control, instrumentation, digital filtering, and frequency synthesis. When used with an up/down counter and control logic, they can be used to perform such operations as multiplication, addition, subtraction, generation of algebraic equations and differential equations, integration, and to raise numbers to various powers. This Note discusses each of these applications and symmetric rate multiplication, the problem of eliminating round-off in a direct frequency-synthesis application in a common-carrier multiplex system.

Rate-Multiplier Description

The rate multiplier is a circuit that produces an output pulse train whose frequency is proportional to the product of two inputs. One of the inputs is a clock frequency, f_c , and the other a pre-programmed multiplier number (binary or BCD) whose value is fixed at a given instant. The output of the rate multiplier is a frequency whose average rate is equal to $f_c x$, where $0 < x \leq 1$. Thus the output rate is always less than or equal to f_c , and, in general, is composed of pulses which are unevenly spaced. It should be noted that even though the output rate is time averaged to the correct fractional rate of the input, there is always a round-off error associated with the output. This error can be reduced by increasing the bit capacity of the multiplier.

The principle of rate multiplication may be illustrated with the aid of the simplified circuit of a binary rate multiplier shown in Fig. 1(a). Four bits of binary information are used to perform multiplication by any factor from $1/16$ to $15/16$ by programming the S_4, S_3, S_2 , or S_1 gates for the proper factor. The final output frequency, f_x , is obtained by ORing the outputs of each AND gate as shown in the figure. The timing diagram in Fig. 1(b) shows how a value for $f_x = \left(\frac{6}{16}\right) f_c$ can be obtained by gating the S_4 and S_2 outputs.

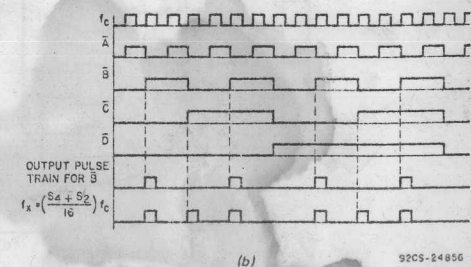
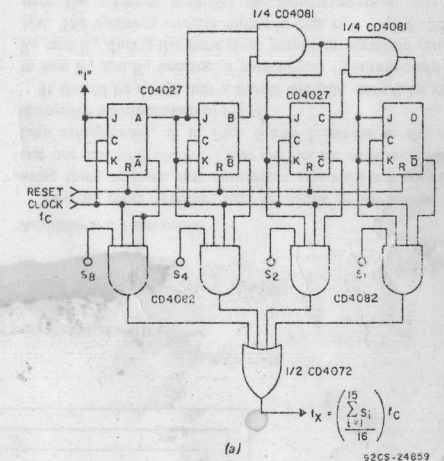


Fig. 1—(a) Simplified circuit of binary rate multiplier; (b) timing diagram for (a).

The functional diagram of the CD4527B (BCD rate multiplier) is shown in Fig. 2. The BCD inputs can be

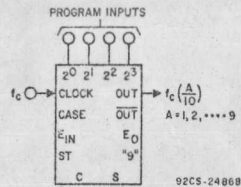


Fig. 2-Functional diagram of the CD4527B, BCD rate multiplier.

programmed from 1 to 9 to form an output multiplier constant of 1/10 to 9/10. For example, if the BCD input were set to seven (0111), the output rate would be $f_c (7/10)$. This multiplication factor can be expanded to a greater number of bits by using the cascade/enable feature of the CD4527B as demonstrated in Fig. 3. The strobe feature

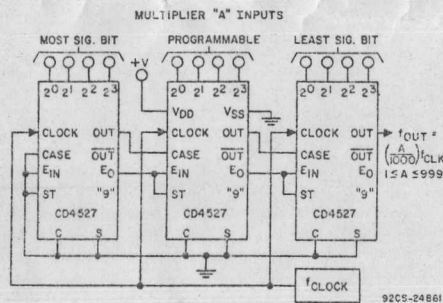


Fig. 3-BCD rate multiplier cascaded for multiplier A/1000, $1 \leq A \leq 999$.

allows outputs to be enabled or inhibited.¹

RATE-MULTIPLIER APPLICATIONS

Cascading

The rate multiplier can be connected in parallel or series as shown in Figs. 3 and 4. When devices are connected in parallel, as in Fig. 3, an n-bit rate multiplier is formed which obeys the input/output relation:

$$f_{out} = \frac{A}{K^n} f_{clk}$$

$$\text{where } 0 < \frac{A}{K^n} < 1$$

In the case of the CD4527B (BCD), the K^n factor is $(10)^n$, where n denotes the number of stages; for the CD4089B (binary), K^n becomes $(2)^n$, where n denotes the number of bits.

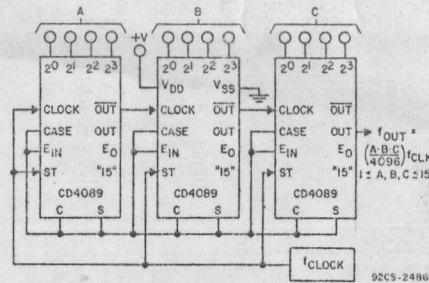


Fig. 4-Multiplication of three variables, A, B, and C.

In the circuit of Fig. 3, three BCD rate multipliers are connected in parallel; they produce an output rate which is proportional to the input clock by any multiple of A/1000. The A variable can be made to assume any value from 1 to 999 by programming the BCD inputs. By using the CD4089B, the same circuit could be used to build a binary multiplier. The variable A would then range from 1 to 4095, and K^n would be $(2)^{12}$ or 4096.

When rate multipliers are arranged serially, as shown in Fig. 4, two or more variables can be multiplied. The input/output relationship for the circuit shown in Fig. 4 is:

$$f_{out} = \frac{A \cdot B \cdot C}{4096} f_{clk}$$

where $1 \leq A, B, \text{ or } C \leq 15$.

Multiplication

Two or more variables can be multiplied by using three or more rate multipliers and one up/down counter. The output is then a fixed number, either BCD or binary, not a pulse rate or frequency as before. Thus, in this discussion, as well as in the following arithmetic applications, the output is referred to as N ($N = 1, 2, \dots$) and not f_{out} .

As an example, consider the circuit shown in Fig. 5. The input variables, A and B, are programmed to a BCD or binary number; the resultant output from the counter (Q_1, Q_2, Q_3, Q_4) is $N = (A \cdot B)/K$. For the CD4527B, $K = 10$, and for the CD4089B, $K = 16$. Since the output of the up/down counter must be an integer from 1 to 9, $A \cdot B/K$ must also be an integer. For example, if $K = 10$, $A = 0101$, and $B = 0100$, then $N = 5(4/10) = 2 = 0010$ as read on the Q_4, Q_3, Q_2 , and Q_1 lines, respectively. Analysis of the circuit of Fig. 5 shows that:

$$R_1 = f_{clk} \left(\frac{A}{10} \right)$$

$$R_2 = f_{clk} \left(\frac{A}{10} \right) \left(\frac{B}{10} \right) = f_{clk} \left(\frac{A \cdot B}{100} \right)$$

$$R_3 = f_{clk} \left(\frac{N}{10} \right)$$

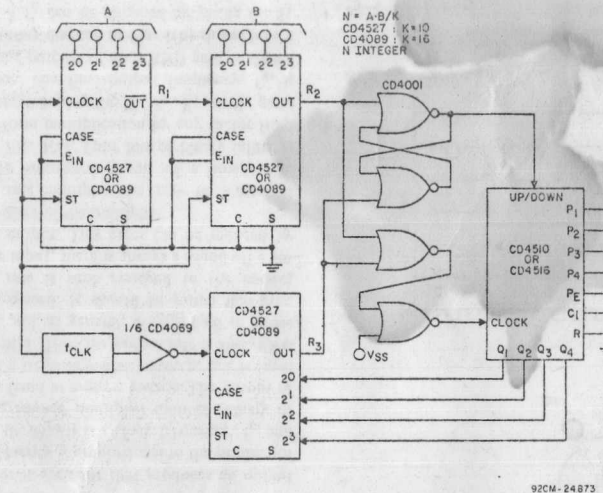


Fig. 5-Multiplication of two variables, A and B.

The interface circuit (CD4001A) shown preceding the up/down counter in Fig. 5 is used to convert the counter from a single clock to a dual-clock input device. Since the counter must count both up and down at random intervals it is desirable to have separate inputs for the up and down commands. The counter cannot accept simultaneous inputs to the command terminal, therefore, a multi-phase clock frequency is used at the input.

In Fig. 5 the output rate, R_2 , addresses the "up count", and R_3 addresses the "down count" of the CD4510B or CD4516B. As R_2 and R_3 change, the counter steps up or down until the loop stabilizes; thus the counter acts as a null detector, equalizing the input rates so that $R_2 = R_3$ when stability is reached. Then, at equilibrium:

$$R_2 = R_3$$

or

$$f_{clk} \left(\frac{A \cdot B}{100} \right) = f_{clk} \left(\frac{N}{10} \right)$$

therefore

$$N = \left(\frac{A \cdot B}{10} \right)$$

If the true product $A \cdot B$ is desired, then another rate multiplier can be used in the feedback loop to eliminate the 1/10 scaler multiplier. When the rate multiplier is programmed for a multiplier of 1, $R_3 = f_{clk} \left(\frac{N}{100} \right)$; thus, $R_2 = R_3$ yields $N = A \cdot B$.

Addition and Subtraction

Two or more variables can be added or subtracted by using three or more rate multipliers, one up/down counter, and one summing circuit. These circuits are constructed in a loop arrangement, as in Figs. 6 and 7, similar to the one shown for multiplication in Fig. 5.

It should be noted that a simple OR gate cannot be used to sum R_1 and R_2 because, if pulses occur simultaneously on R_1 and R_2 during the same clock period, information can be lost. The summing circuits shown in Figs. 6, 7, and 8 eliminate the problem provided the synchronization rate is higher than that of R_1 and R_2 .

Fig. 6 is the diagram of a circuit used to sum two variables, A and B. The figure shows that R_1 and R_2 are summed and routed to the "up count" terminal of the counter. In subtraction, the summing circuit is placed in the signal path to the "down count" terminal of the counter, as illustrated in the circuit of Fig. 7. Both addition and subtraction can be performed.

In Fig. 6:

$$R_3 = R_1 + R_2 = f_{clk} \left(\frac{A}{10} \right) + f_{clk} \left(\frac{B}{10} \right)$$

$$R_4 = f_{clk} \left(\frac{N}{10} \right)$$

Then, at equilibrium:

$$R_3 = R_4$$

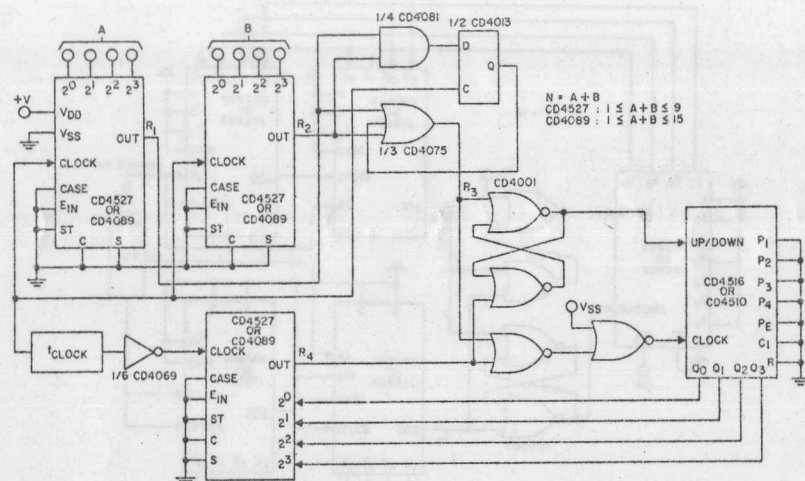


Fig. 6—Addition of two variables, A and B.

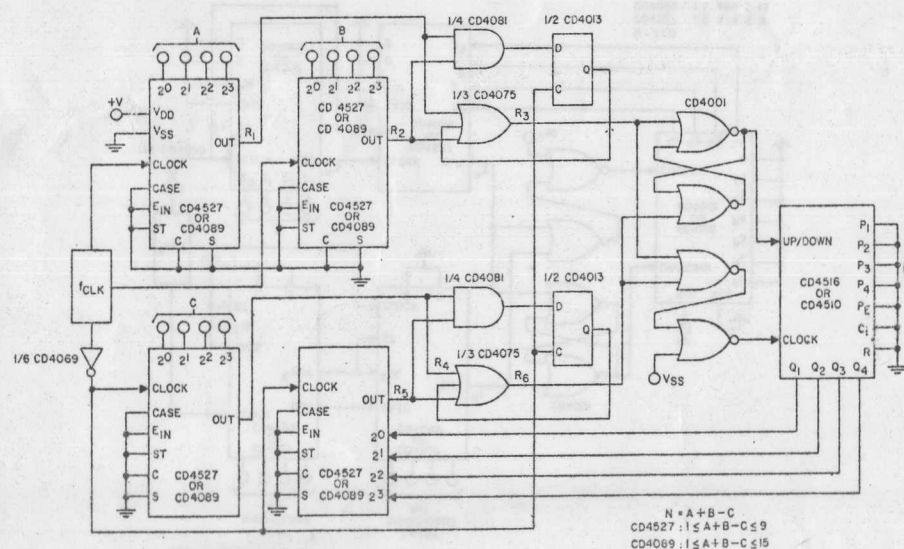


Fig. 7—Combined addition and subtraction.

therefore

$$f_{\text{clk}} \left(\frac{A}{10} \right) + f_{\text{clk}} \left(\frac{B}{10} \right) = f_{\text{clk}} \left(\frac{N}{10} \right)$$

or

$$N = A + B$$

As discussed above, the circuit shown in Fig. 7 is used to add and subtract simultaneously. From Fig. 7:

$$R_3 = R_1 + R_2 = f_{\text{clk}} \left(\frac{A}{10} \right) + f_{\text{clk}} \left(\frac{B}{10} \right)$$

$$R_6 = R_4 + R_5 = f_{\text{clk}} \left(\frac{C}{10} \right) + f_{\text{clk}} \left(\frac{N}{10} \right)$$

Then, at equilibrium:

$$R_3 = R_6$$

and

$$N = A + B - C$$

Finally, the average-rate output of the rate multiplier can be modified by the sum of two variables by using the less complex circuit shown in Fig. 8. It should be noted that the output is a time-averaged rate, not a fixed number, N, as before.

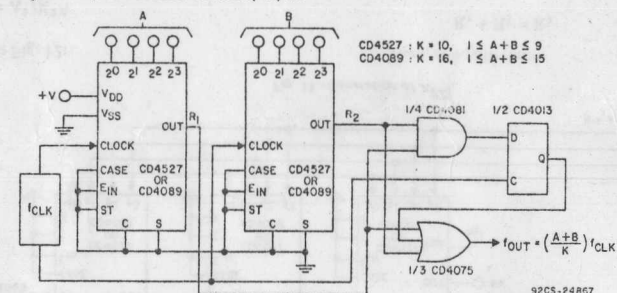


Fig. 8—The sum of two variables, A and B, with a constant multiplier.

Division

Two variables, A and B, can be divided by use of the circuit shown in Fig. 9. Two rate multipliers are connected in parallel to form the A variable. The parallel connection ensures that the multiplier constant, 1/10, does not appear in the final result, A/B. From Fig. 9:

$$R_1 = f_{\text{clk}} \left(\frac{A}{100} \right)$$

$$R_2 = f_{\text{clk}} \left(\frac{B}{10} \right)$$

$$R_3 = R_2 \left(\frac{N}{10} \right) = f_{\text{clk}} \left(\frac{N}{10} \right) \left(\frac{B}{10} \right)$$

At equilibrium, $R_1 = R_3$; therefore:

$$\frac{A}{100} = \left(\frac{N}{10} \right) \left(\frac{B}{10} \right)$$

or

$$N = \frac{A}{B}$$

Square Roots/Higher-Order Roots/Algebraic Equations

The RCA COS/MOS rate multiplier can be used in circuits such as those shown in Figs. 10 and 11 to generate roots of the form $A^{x/y}$, where x and y are integers. The up/down counter is also used in a feedback loop configuration, as in Figs. 5 through 8, above, to perform this operation. The counter is also used in a feedback loop configuration, as in Figs. 5 through 8, to perform this operation. The variable A and the other two with unity.

From Fig. 10:

$$R_1 = f_{\text{clk}} \left(\frac{1}{10} \right) \left(\frac{A}{10} \right) = f_{\text{clk}} \left(\frac{A}{100} \right)$$

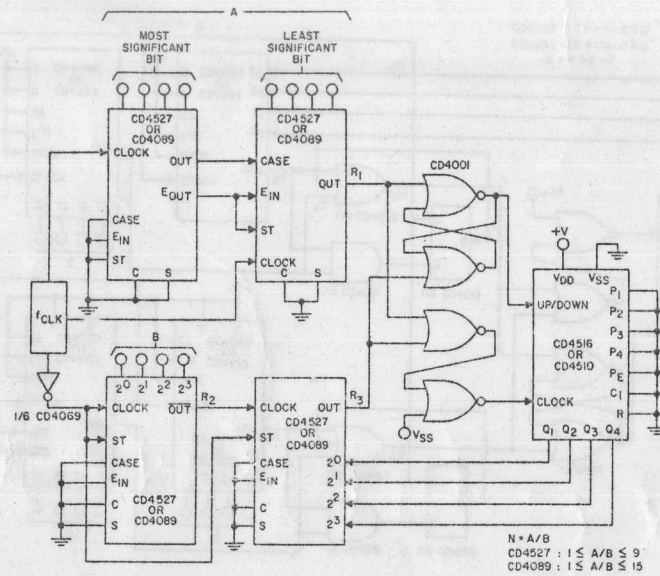
$$R_2 = f_{\text{clk}} \left(\frac{N}{10} \right) \left(\frac{N}{10} \right) = f_{\text{clk}} \left(\frac{N^2}{100} \right)$$

Then, at equilibrium:

$$R_1 = R_2$$

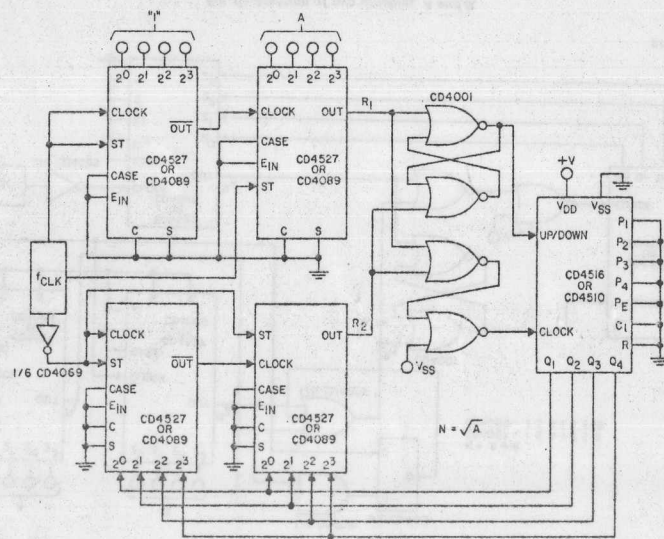
therefore

$$N = \sqrt{A}$$



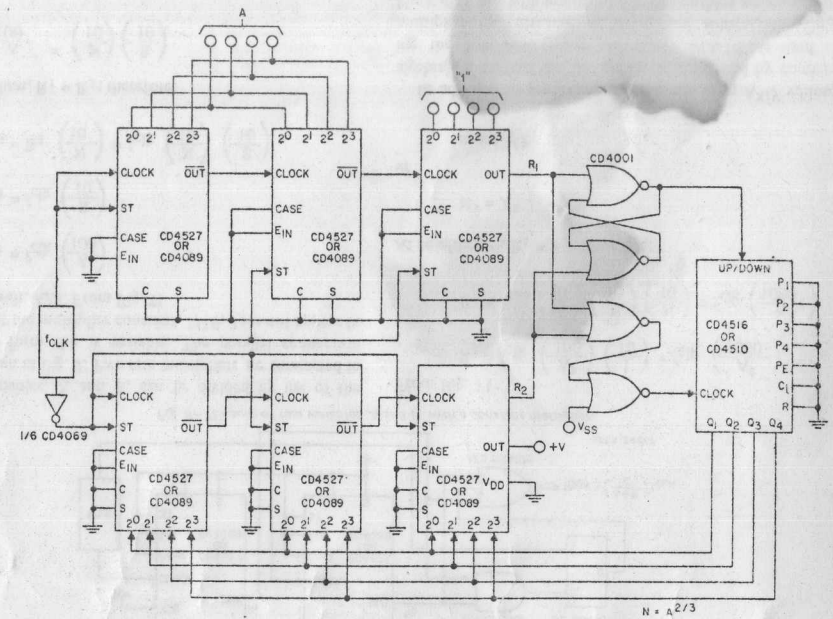
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Fig. 9—Division of the variable A by the variable B.



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Fig. 10—Generation of $A^{1/2}$.



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Fig. 11—Generation of $A^{2/3}$.

From Fig. 12:

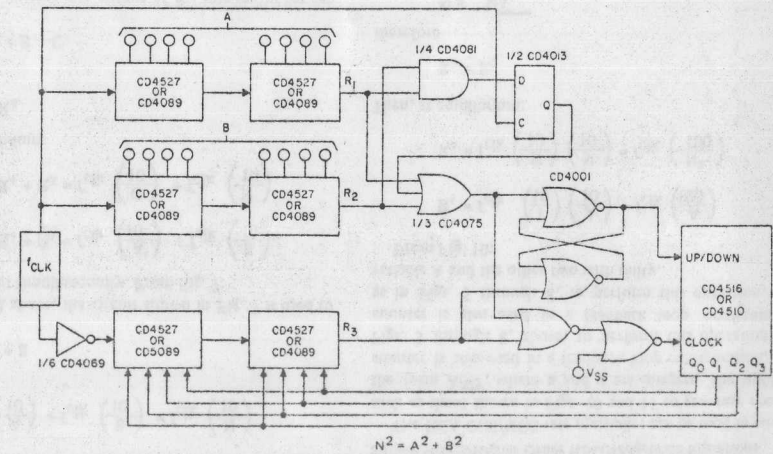
$$\begin{aligned} R_1 &= A^2/K^2n \\ R_2 &= B^2/K^2n \\ R_3 &= N^2/K^2n \end{aligned}$$

Then, at equilibrium:

$$R_1 + R_2 = R_3$$

therefore,

$$N^2 = A^2 + B^2$$



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Fig. 12—Generation of the equation $N^2 = A^2 + B^2$.

The COS/MOS CD4527B and CD4089B rate multipliers can also be used to solve equations. For example, Fig. 13 can be used to solve the well-known quadratic equation,

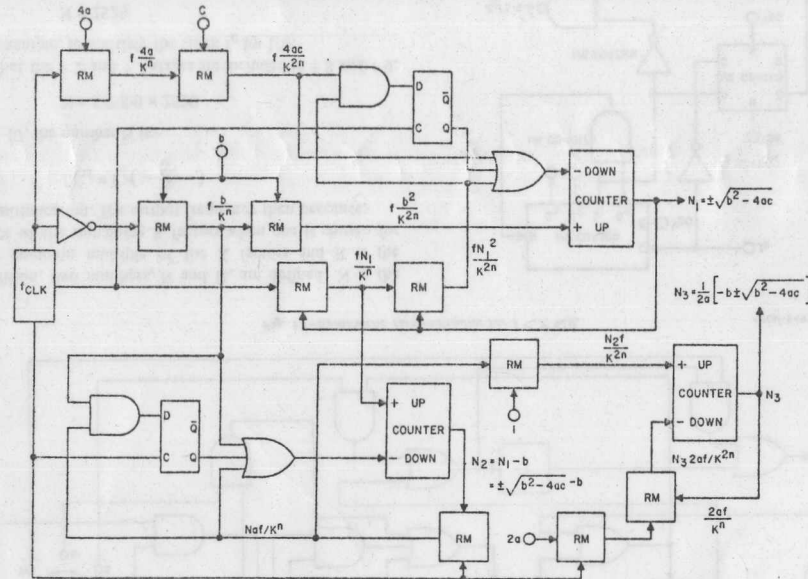


Fig. 13—Solutions of the quadratic equation, $ax^2 + bx + c$.

$ax^2 + bx + c = 0$. The solutions, x_1 and x_2 , are assumed to be real, and can be found by monitoring the output of counter N_3 . As discussed above, the K^n , K^{2n} factors are the multiplication factors inherent with the type of rate multiplier (BCD or binary) used.

Frequency Ratios

The circuit shown in Fig. 14 can be used to compute the ratio of two frequencies, f_1 and f_2 . Since the frequencies are usually random, care should be taken to condition these inputs to ensure that coincidence does not occur at the counter command input. Fig. 15 shows a circuit that can be used to condition the input frequencies.⁴ The input clock frequency should be at least 4 times faster than the highest input frequency (f_1 or f_2).

From Fig. 14:

$$R_1 = f_1/K^n$$

and

$$R_2 = f_2/N/K^n$$

Then, at equilibrium, $R_1 = R_2$; therefore:

$$N = f_1/f_2$$

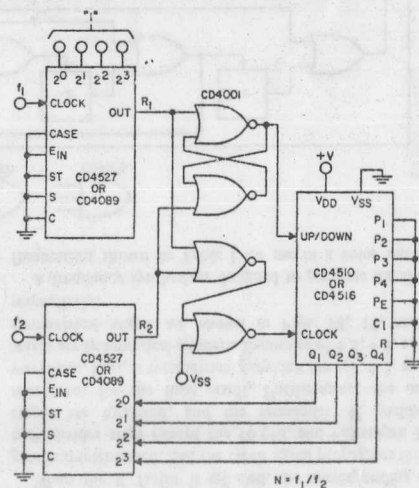


Fig. 14—Frequency ratios.

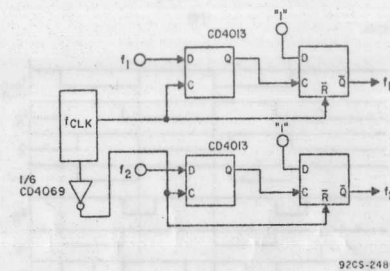


Fig. 15—Retiming circuit for f_1 and f_2

Integration

The CD4527B and CD4089B rate multipliers can be used as digital integrators by feeding the output of the rate multiplier to the input of an up/down counter in the up-count mode only. The system will operate as an integrator if the input to the counter is in pulse form. Each pulse input to the counter acts as an increment with respect to time, and the counter accumulates these increments. If the counter is large enough, so that the delta increment represents only a small portion of the total counter contents, then the delta increment approaches a differential and the counter accumulates the integral of this differential over time. For example, assume that the counter output is $N(\mu)$ where μ represents the 'incremental pulse and is monotonically increasing. If each pulse at the input to the rate multiplier increases μ by one unit, and the frequency f is defined as $f = d\mu/dt$, then the output of the rate multiplier is:

$$K \frac{d\mu}{dt} = Kf_{clk}$$

This relation is the same as that described above under the heading "Rate Multiplier Description".

If the output of the rate multiplier is supplied to the up-count input of the counter, then, at a given instant:

$$K \frac{d\mu}{dt} = N(\mu)$$

But the counter output $N(\mu)$ is changing with time owing to its input $K \frac{d\mu}{dt}$, thus:

$$K \frac{d\mu}{dt} = \frac{dn}{dt}$$

or

$$Kd\mu = dn$$

Therefore

$$N(\mu) = \int_0^{\mu} Kd\mu$$

Fig. 16 illustrates the principle of integration as described above. If the feedback loop scheme is used in Fig. 16 i.e., if $N(\mu)$ is the program input A to the multiplier:

$$N(\mu) = \int_0^{\mu} Kd\mu = \int_0^{\mu} \frac{A}{K^n} d\mu = A$$

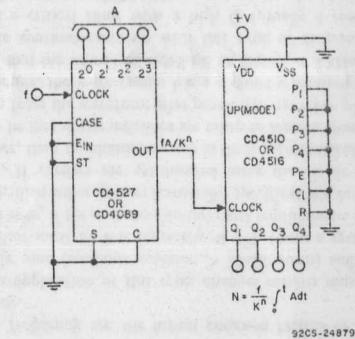


Fig. 16—Integration.

Therefore

$$\frac{dA}{d\mu} = \frac{1}{K^n} \mu$$

or

$$A = e^{\mu/K^n}$$

Thus, the rate multiplier can also be used to solve differential equations.

Symmetric Rate Multiplication

In the previous discussion, the classic rate multiplier was used to produce an output pulse train whose period is not generally symmetrical. In many cases, the multiplication factor $1/K$ is not of the form $1/2^n$ (n integer); thus, a "round off" error is associated with the output signal. In fact, if the output waveform is observed on a spectrum analyzer, a Bessel distribution similar to that caused by an FM modulated signal will appear. In many applications where spectral purity is important, such harmonic and spurious outputs are intolerable.

There is a technique, the symmetric rate multiplication technique (SRM), that can be used to eliminate rate outputs with the above mentioned spectral characteristics. The SRM approach yields output rates with symmetrical duty cycles (50 percent) and no "round off" errors. The only limitation to the SRM technique is the clock frequency. However, in applications where limited numbers of frequencies are to be synthesized, the SRM approach works very well, and the clock or master oscillator is not a controlling factor.

Consider the circuit shown in Fig. 17, where the input clock frequency f_c is derived from an oscillator whose period is symmetrical (50-percent duty cycle) and whose frequency is fixed. For simplicity, the multiplication factors programmed in are of the form $1/K$, where $1 \leq K \leq 9$. The final output frequency is:

$$f_{out} = f_c \left(\frac{1}{K} \right)$$

where f_{out} is a frequency whose period is symmetrical. The multiplication factors $1/K$ are assumed to be available and stored for use at any given time as they are in the CD4527B.

When the K factor is selected, the corresponding AND gate is implemented, and the clock signal propagates through each divider stage except the $\div 6$ ($\div 3$, and $\div 2$) stages. These stages are bypassed, and the remainder, R , yields the numerator for the final result. Furthermore, the output waveform, f_{out} , is symmetrical provided the $\div 3$, $\div 5$, and $\div 7$ stages are symmetrical dividers. Examples of $\div 3$, $\div 5$, and $\div 7$ symmetrical stages are shown in Figs. 18, 19, and 20, respectively.

A frequency synthesizer designed to generate the channel frequencies shown in Table I for use in a voice multiplex

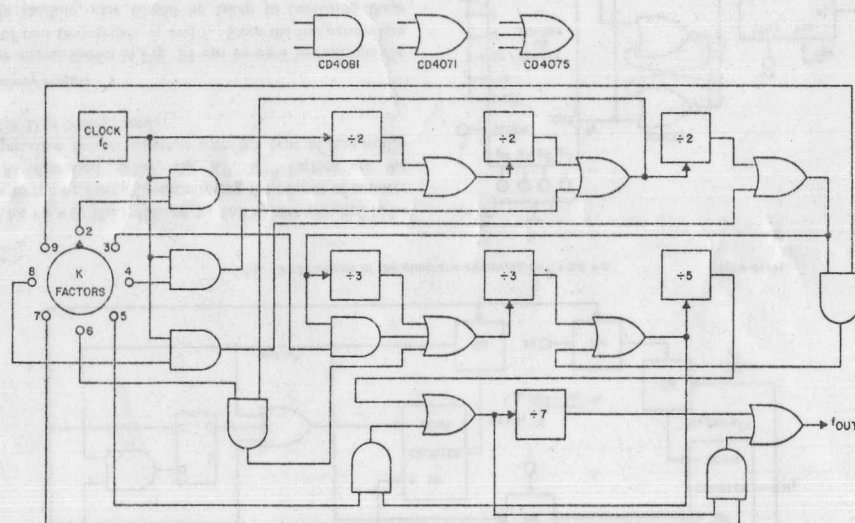


Fig. 17—Symmetric rate multiplier for $1 < K \leq 9$.

In addition, two numbers, N and R , are defined: N is the lowest common multiple of the K factors and R is the product of the remaining K factors when one is chosen for rate multiplication. The output frequency then becomes:

$$f_{out} = f_c \left(\frac{R}{N} \right)$$

In Fig. 17, the number N is:

$$N = 5 \cdot 7 \cdot 8 \cdot 9 = 2520$$

Note that the $\div 2$ and $\div 3$ stages are included in $\div 8$ and $\div 9$. As an example, to multiply the clock f_c by $1/6$:

$$N = 2520$$

$$R = 2 \cdot 2 \cdot 3 \cdot 5 \cdot 7$$

and

$$f_{out} = f_c \left(\frac{2 \cdot 2 \cdot 3 \cdot 5 \cdot 7}{2520} \right) = f_c \left(\frac{1}{6} \right)$$

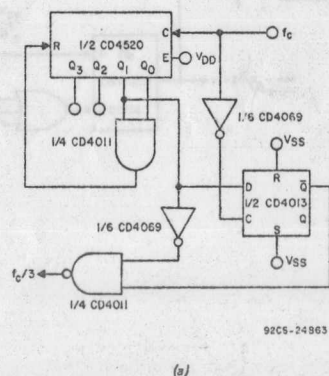


Fig. 18—(a) Symmetrical $\div 3$ and (b) timing diagram.

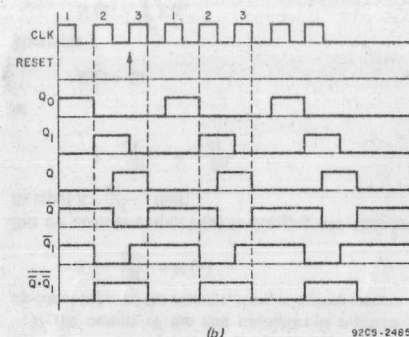


Fig. 18—(a) Symmetrical $\div 3$ and (b) timing diagram.

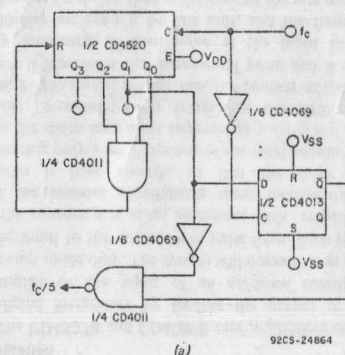


Fig. 19—(a) Symmetrical $\div 5$ and (b) timing diagram.

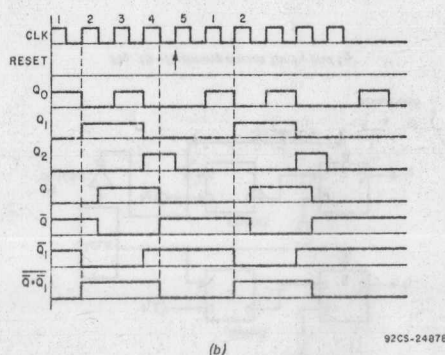


Fig. 19—(a) Symmetrical $\div 5$ and (b) timing diagram.

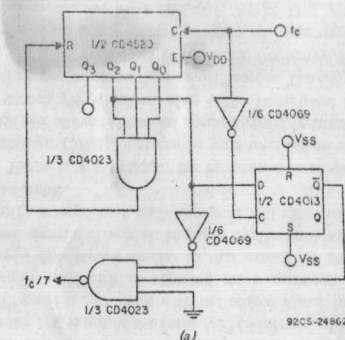


Fig. 20—(a) Symmetrical $\div 7$ and (b) timing diagram.

system up through the first (CCITT) group will demonstrate the SRM technique. The numbers listed next to each channel frequency are the lowest common factors of that frequency.

In an application of this type, channel carriers must be spectrally pure (spurious emission > 70 -dB down) and the phase jitter must be low (typically $\leq 1^\circ$). From a systems point of view, if these carriers do not meet requirements such as these, then other system (crosstalk) specifications cannot be met. If carriers are synthesized using the classic rate multiplier, then requirements such as those mentioned above will not be met unless measures are taken to remove spurious emission from the waveform after generation has taken place. For example, the voice carrier has a channel separation of 4 kHz, so that the unwanted sideband separation is 8 kHz. To eliminate spurious emission with this type of distribution requires a critical filter with a high Q (usually 4 coils, 9 poles). Suppression of FM jitter or noise is another problem altogether. The SRM approach minimizes these problems because:

1. Output frequencies synthesized by the SRM technique have 50-percent duty cycles; thus, only odd harmonics exist, and these are easy to filter out.
2. The output has been derived from divider chains; thus, FM suppression by factors of $20 \log N$ will exist. For example, a $\div 2$ yields $20 \log 2$ or approximately 6 dB of suppression.

Table I indicates that dividers ranging from 2 to 31 are needed to synthesize the 28 carriers listed. To synthesize these frequencies, a clock whose LCM (lowest common multiple) is that of the desired frequencies is chosen; as described above,

Table I — Channel Frequencies

Channel Freq. (kHz)	Lowest Common Factors (Divider Stages)
28	2, 2, 7
32	2, 2, 2, 2, 2
36	2, 2, 3, 3
40	2, 2, 2, 5
44	2, 2, 11
48	2, 2, 2, 2, 3
52	2, 2, 13
56	2, 2, 2, 7
60	2, 2, 3, 5
64	2, 2, 2, 2, 2, 2
68	2, 2, 17
72	2, 2, 2, 3, 3
76	2, 2, 19
80	2, 2, 2, 2, 5
84	2, 2, 3, 7
88	2, 2, 2, 11
92	2, 2, 23
96	2, 2, 2, 2, 2, 3
100	2, 2, 5, 5
104	2, 2, 2, 13
108	2, 2, 3, 3, 3
112	2, 2, 2, 2, 7
116	2, 2, 29
120	2, 2, 2, 3, 5
124	2, 2, 31
128	2, 2, 2, 2, 2, 2, 2
132	2, 2, 3, 11
136	2, 2, 2, 17

Table II — Channel Carriers Synthesizable with Clock Frequencies Not Exceeding 10 MHz

Channel Frequency (kHz)	Lowest Common Factors (Divider Stages)
32	2, 2, 2, 2, 2
36	2, 2, 3, 3
40	2, 2, 2, 5
48	2, 2, 2, 2, 3
60	2, 2, 3, 5
64	2, 2, 2, 2, 2, 2
72	2, 2, 2, 3, 3
80	2, 2, 2, 2, 5
96	2, 2, 2, 2, 2, 3
120	2, 2, 2, 3, 5
128	2, 2, 2, 2, 2, 2, 2
28	2, 2, 7
44	2, 2, 11
56	2, 2, 7
84	2, 2, 3, 7
88	2, 2, 2, 11
112	2, 2, 2, 2, 7
132	2, 2, 3, 11
52	2, 2, 13
68	2, 2, 17
104	2, 2, 2, 13
136	2, 2, 2, 17

Clock = 5,760 kHz
LCM = $128 \cdot 9 \cdot 5 = 5,760$

Clock = 3,696 kHz
LCM = $7 \cdot 11 \cdot 16 \cdot 3 = 3,696$

Clock = 1,768 kHz
LCM = $8 \cdot 13 \cdot 17 = 1,768$

SUMMARY

The COS/MOS rate multipliers CD4527B and CD4089B can be used to generate many digital functions. These MSI circuits are very useful as basic building blocks in low-power systems where minimum package count is desirable. Several of these applications, such as frequency synthesis and instrumentation, require low power and low package count to be competitive. Many arithmetic functions can also be performed by the COS/MOS rate multipliers with the aid of an up/down counter and some control logic. This feature is very useful in several areas of numeric control and digital processing systems. All of these features, and the fact that the CD4527B and CD4089B are part of the standard COS/MOS family of digital IC's, make these devices very useful to the design engineer.

REFERENCES AND BIBLIOGRAPHY

1. A more detailed analysis of the cascade, strobe, E_O , E_{IN} , and "9" or "15" features can be found in the CD4527 or CD4089 data sheets.
2. RCA DATABOOK Series SSD-203B, "COS/MOS Digital Integrated Circuits," 1975.
3. A. R. Elliott, "A High-Speed Binary Rate Multiplier," Proceedings of the IEEE, August 1971, pp. 1256-1257.
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6. K. P. Rajappan, V.C.V. Pratapa Reddy, "Decade Rate Multiplier," Proceedings Letters, February 1972, pp. 759.
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the limiting factor of the SRM approach is the clock frequency. The table shows that the clock frequency increases as the number of frequencies to be synthesized increases. COS/MOS circuitry is used in this example, and since a COS/MOS device normally operates at 10 MHz, f_{clk} will not exceed this frequency. Table II lists some of the many combinations that can be used to obtain channel carriers that can be synthesized with clock frequencies not exceeding 10 MHz; those not listed can be obtained by a number of clock frequency choices. Using Table II, circuits similar to those shown in Fig. 17 can be constructed to implement this application.

Many possible LCM combinations can be used to implement the SRM technique, as illustrated; however, the common factors (dividers) must be bypassed in the synthesized frequency, and remainder (R dividers) used to obtain the final result. For example, when 72 kHz is to be synthesized, the $\div 2$, $\div 2$, $\div 2$, $\div 3$, and $\div 3$ factors are bypassed and the $\div 2$, $\div 2$, $\div 2$, $\div 2$, $\div 3$, and $\div 5$ remainder used.

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices", Form No. 1CE-402, available on request

